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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/729.622
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		First Named Inventor	Narayanan Krishnamurthy
		Group Art Unit	2825
		Examiner Name	GARBONSKI
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W	AA	Burch et al., "Sequential Circuit Verification Using Symbolic Model Checking," 27th ACM/IEEE Design Automation Conference, 1990, Paper 3.2, pp. 46-51.	
N	AB Cabodi et al., "Symbolic FMS Traversals Based on the Transition Relation," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 16, No. 5, May 1997, pp. 448-457.		
W	AC	Touati et al., "Implicit State Enumeration of Finite State Machines using BDD's," IEEE ICCAD, November 1990, pp. 130-133.	

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